The **Erlangen National High Performance Computing Center** (NHR@FAU) is looking for a

Bachelor/Master thesis student for

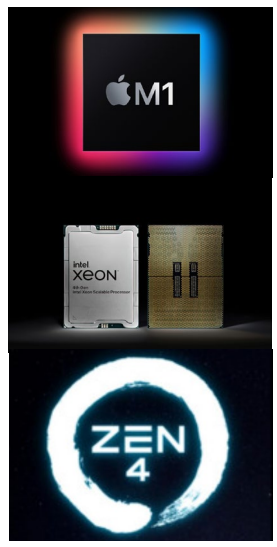
Development and in-core Performance Analysis with OSACA (Python/Assembly)

The thesis will be supervised by and conducted in the Research division at NHR@FAU, led by Prof. Dr. Harald Köstler.

Description

The Open-Source Architecture Code Analyzer (OSACA, https://go-nhr.de/OSACA) is a tool developed at our team for static in-core analysis of assembly code snippets. This allows the user to predict the performance of innermost loops and incorporate these results into a system-wide performance model for analysis or optimization. It supports various x86 Intel and AMD micro-architectures, as well as a variety of ARM-based µ-archs.
In this thesis you will develop a thorough understanding of modern microarchitectures and their out-of-order execution of code. You will apply this knowledge for enhancing the current implementation of OSACA in various directions based on your personal preferences and skill set. You will verify new findings and reverse-engineering on real bleeding-edge hardware and identify bottlenecks via careful benchmarking.

Within the thesis, the focus of work includes a subset of the following areas (will be determined in discussion between the student and the advisor based on personal interest and feasibility):



- Getting familiar with the OSACA tool, its usage, and its code structure (Python)
- Object-oriented code refactoring of existing code
- Performance optimizations of modern Python code (DB access, graph analysis, parallelization)
- Enhancement of the current feature set, e.g.:
  - Intel assembly syntax support
  - Frontend consideration during analysis (instruction decoding/dispatching/ retirement, register file, LSB, …)
  - Support of a “timeline view”, i.e., simulator-like analysis of code loops
  - Enhanced latency modeling (including excessive micro-benchmarking)
- Development of an ISA-independent micro-benchmark harness for identifying port utilizations of instructions
- Develop in-core performance models for new architectures, e.g., Intel Sapphire Rapids, AMD Zen 4, or Apple M1
- Running the benchmarks on NHR@FAU’s 5-Petaflop Top500-class “Fritz” supercomputer

Working on these topics, you will have the chance to work with **state-of-the-art supercomputing technology** in a scientific environment. We foster **scientific thinking** and proper **data presentation skills**.

Required skills

- Profound knowledge of Python
- Preferably knowledge of Assembly language(s)
- Knowledge of basic performance modeling strategies (e.g., Roofline)
- Excellent communication skills in English and/or German

Please direct any inquiries or applications to

Jan Laukemann <jan.laukemann@fau.de>
Georg Hager <georg.hager@fau.de>
Gerhard Wellein <gerhard.wellein@fau.de>